HETEROJUNCTION TYPE COMPOUND SEMICONDUCTOR FIELD EFFECT TRANSISTOR AND ITS MANUFACTURING METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2002-358337, filed Dec. 10, 2002, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a semiconductor device, for example, heterojunction type compound semiconductor field effect transistor and its manufacturing method.

[0004] 2. Description of the Related Art

[0005] In recent years, much attention has been paid to high-frequency compound semiconductor field effect transistors utilizing heterojunctions. These high-frequency field effect transistors are produced by stacking and processing compound semiconductor layers on a compound semiconductor substrate made of GaAs or the like. They are applied to high-power amplifiers, switches, low-noise amplifiers, and the like. In particular, if the high-frequency field effect transistor is applied to a high-power amplifier, it must have a high withstanding voltage and offer a low parasitic resistance. The field effect transistor that must have a high withstanding voltage and offer a low parasitic resistance often employs a structure called "double recess". The double recess structure is a technique by which a contact layer is formed of a two-stage recess in order to ensure a sufficient withstanding voltage while reducing the parasitic resistance. In the double recess structure, the depths of a first recess opening (wide recess opening) and a second recess opening (narrow recess opening) determine the characteristics of the field effect transistor such as its maximum drain current and mutual conductance. Accordingly, when a two-stage recess is formed, it is important to properly control the depths of the first and second recess openings in order to obtain a high yield. Thus, a recess etching process must be very accurate. Further, it is necessary that the recess etching process does not cause a substrate damage that may degrade the characteristics of the transistor. For example, Jpn. Pat. Appln. KOKAI Publication No. 7-335867 discloses a wet etching method utilizing differences in etching speed among materials.

[0006] **FIG. 1** shows the sectional structure of a conventional heterojunction type field effect transistor. This field effect transistor comprises a semi-insulating GaAs substrate **111** and a buffer layer **112**, an electron supply underlayer **113** composed of AlGaAs doped with n type impurities, a semiconductor channel layer **114** composed of undoped GaAs or InGaAs, an electron supply layer **115** composed of AlGaGs doped with n type impurities, a contact underlayer **116** composed of n-InGaP doped with n type impurities, and a contact overlayer **117** composed of GaAs doped with n type impurities, all the layers being sequentially stacked on the substrate **111**. A wide recess opening is formed so as to penetrate the contact overlayer **117**. A narrow recess opening **132** is formed inside the wide recess opening so as to penetrate the contact underlayer **116**. A gate electrode **122** is formed on a surface of the electron supply layer **115** exposed from the bottom of the narrow recess opening. A source electrode **120** and a drain electrode **121** are formed on a surface of the contact overlayer **117** so that the wide recess opening is sandwiched between them.

[0007] In the prior art, to accurately form such a double recess structure, an etching operation is performed on the basis of a marked difference in selectivity between etchants used for recess etching, i.e. whether each etchant selectively etches the material InGaP or the material GaAs or InGaAs. For example, an H_3PO_4 (phosphoric acid)-based etchant etches InGaAS or GaAs but does not substantially etch InGaP. On the other hand, an HCL (hydrochroic acid)-based etchant does not substantially InGaAS or GaAs, but significantly etches InGaP. That is, when the GaAs contact overlayer **117** is etched by first recess etching using an H_3PO_4-based etchant, the etching substantially stops at the surface of the GaAs contact overlayer **117**. Then, when the InGaP contact underlayer **116** is etched by second recess etching using an HCl-based etchant, the etching substantially stops at the surface of the AlGaAs electron supply layer **115**, formed under the InGaP contact underlayer **116**. Thus, the first recess etching and second recess etching are controlled.

[0008] In the conventional heterojunction type compound semiconductor field effect transistor, electrons supplied by the source electrode **120** flow through the contact over layer **117**, composed of n^+-GaAs and offering low resistance, and then through the n-InGaP contact underlayer. The electrons then flow through the channel layer **114**, again through the n-InGaP underlayer **116**, and through the low-resistance contact overlayer **117** into the drain electrode **121**.

[0009] However, InGaP, constituting the contact underlayer, has a lower electron mobility than GaAs and InGaAs. For example, the mobility of n-GaAs is 1,700 $cm^2V^{-1}s_{-1}$ at a concentration of 5×10^{18} cm^{-3}, whereas the mobility of n-InGaP is 800 $cm^2V^{-1}s_{-1}$ at a concentration of 2×10^{18} cm^{-3}. To exhibit an excellent ohmic characteristic, the n^+-GaAs contact overlayer **117**, which contacts directly with the source electrode **120** and the drain electrode **121**, is doped with a high concentration of n type impurities so as to offer a low resistance. Thus, the resistance value of the contact underlayer **116** significantly affects parasitic resistance such as the source resistance of the transistor.

[0010] In the above described configuration, electrons must flow through the n-InGaP contact underlayer **116**, having a low electron mobility. This disadvantageously increases the parasitic resistance of the transistor. An increase in the parasitic resistance of the transistor reduces the mutual conductance or maximum drain current of the transistor. If this transistor is applied to a high-frequency power amplifier, its gain may decrease. If the transistor is applied to a high-frequency switch, its insertion loss may increase.

BRIEF SUMMARY OF THE INVENTION

[0011] According to an aspect of the present invention, a heterojunction type compound semiconductor field effect transistor comprises a channel layer provided on a compound semiconductor substrate and composed of intrinsic GaAs or InGaAs, a first electron supply layer provided on